IN THE CLAIMS:

Please amend the claims as set forth herein:

1. (Currently Amended) A method for fabricating a semiconductor memory device, comprising the steps of:

depositing first and second insulating layers on a semiconductor substrate having ~~where~~ a predetermined shallow trench isolation (STI) region and a predetermined deep trench isolation (DTI) region ~~are defined~~;

forming the STI region by selectively etching the second and first insulating layers and the semiconductor substrate;

forming a photoresist to cover the STI region and expose the predetermined DTI region; ~~curing the surface of the photoresist; and~~

curing a surface of the photoresist by implanting high energy argon ions or through an e-beam process, causing polymers in said photoresist to crosslink and thereby increasing an etch resistance of said photoresist; and

forming the DTI region by using only the cured photoresist and the second insulating layer as a mask.

2. (Currently Amended) The method according to claim 1, wherein the curing step of the photoresist surface includes implanting high energy argon ions into the photoresist with an ion implantation concentration of $10^{12\sim15}$ cm^3, said argon employed only to supply energy to said photoresist.

3. (Currently Amended) The method according to claim 2, wherein an implanting ~~concentration of the argon ions is $10^{12\sim15}$ cm^3 and the implanting~~ energy of the argon ions is 10~200Kev.

4. (Currently Amended) The method according to claim 1, wherein the curing step of the photoresist surface is performed by an e-beam curing process in which high energy electrons are passed through the surface of the photoresist.

5. (Currently Amended) The method according to claim 4, wherein an ~~the~~ energy of the e-beam curing process is 1000~2000uC/cm^2.

6. (Currently Amended) The method according to claim 1, wherein the photoresist formation process includes an exposure process, which selects one light source among i-ray (365nm), KrF (248nm) and ArF(193nm).

7. (Original) The method according to claim 1, wherein the first insulating layer is a pad oxide layer.

8. (Original) The method according to claim 1, wherein the second insulating layer is a pad nitride layer.

9. (Original) The method according to claim 1, wherein the STI region has a depth of 2500~3000Å from the surface of the semiconductor substrate.

10. (Original) The method according to claim 1, wherein the DTI region has a depth of 7000~8000Å from the surface of the semiconductor substrate.